IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A chip-scale package, comprising:

a semiconductor device including an active surface; and

an interposer comprising a semiconductor material and including a first surface disposed adjacent the active surface and including:

solder forming at least one electrically conductive via and a conductive structure protruding from the at least one electrically conductive via at the first surface of the interposer, ~~comprising solder and~~ the at least one electrically conductive via extending at least partially ~~therethrough~~through the interposer, positioned over the semiconductor device, and in communication with a corresponding bond pad of the semiconductor device; and

at least one conductive trace in communication with the at least one electrically conductive via and carried on a second surface of the interposer, opposite from the first surface of the interposer.

2. (Previously presented) The chip-scale package of claim 1, further comprising an electrically conductive bump protruding from the interposer opposite the semiconductor device, in communication with the at least one electrically conductive via, and located at an opposite end of the at least one conductive trace from the at least one electrically conductive via.

3. (Previously presented) The chip-scale package of claim 1, wherein the interposer comprises at least another electrically conductive via that extends substantially directly therethrough.

4. (Canceled)

5. (Previously presented) The chip-scale package of claim 1, wherein a substrate of the semiconductor device and the interposer comprising semiconductor material comprise the same type of semiconductor material.

6. (Previously presented) The chip-scale package of claim 1, wherein a substrate of the semiconductor device and the interposer comprising semiconductor material comprise materials having substantially the same coefficients of thermal expansion.

7. (Previously presented) The chip-scale package of claim 1, wherein a substrate of the semiconductor device comprises silicon.

8. (Previously presented) The chip-scale package of claim 1, wherein the semiconductor material comprises silicon.

9. (Previously presented) The chip-scale package of claim 1, wherein a first thickness of the semiconductor device and a second thickness of the interposer are substantially the same.

10. (Previously presented) The chip-scale package of claim 1, wherein a first thickness of the semiconductor device is greater than a second thickness of the interposer.

11. (Previously presented) The chip-scale package of claim 1, wherein the second surface of the interposer is at least partially coated with an insulative material.

12. (Previously presented) The chip-scale package of claim 11, wherein the insulative material comprises a layer extending substantially over the surface.

13. (Previously presented) The chip-scale package of claim 11, wherein the insulative material comprises an oxide.

14. (Previously presented) The chip-scale package of claim 11, wherein the insulative material comprises silicon oxide.

15. (Previously presented) The chip-scale package of claim 1, further comprising an intermediate layer disposed between the semiconductor device and the interposer.

16. (Previously presented) The chip-scale package of claim 15, wherein the intermediate layer comprises an adhesive material.

17. (Previously presented) The chip-scale package of claim 15, wherein the intermediate layer comprises polyimide.

18. (Previously presented) The chip-scale package of claim 15, wherein the at least one electrically conductive via and the corresponding bond pad communicate through the intermediate layer.

19. (Previously presented) The chip-scale package of claim 1, wherein conductive material of the at least one electrically conductive via is bonded to the corresponding bond pad.

20. (Previously presented) The chip-scale package of claim 1, wherein a contact between the at least one electrically conductive via and the corresponding bond pad comprises a diffusion region comprising a bond pad material and a via material.

21. (Currently amended) A chip-scale package, comprising:
an interposer comprising semiconductor material and including:

a first surface with contact areas arranged correspondingly to an arrangement of bond pads on an active surface of a semiconductor device of the chip-scale package;

solder forming conductive vias that ~~comprise solder~~ extending therethrough and conductive structures protruding from the conductive vias, the conductive vias and conductive structures corresponding to the contact areas; and

a second surface opposite the first surface and carrying at least one conductive trace extending laterally from a conductive via of the conductive vias; and

the semiconductor device invertedly disposed adjacent to the first surface of the interposer so that bond pads of the semiconductor device communicate with corresponding conductive vias of the interposer.

22. (Previously presented) The chip-scale package of claim 21, wherein the bond pads contact the corresponding conductive vias.

23. (Previously presented) The chip-scale package of claim 22, further comprising diffusion regions between the bond pads and the corresponding conductive vias.

24. (Previously presented) The chip-scale package of claim 23, wherein each of the diffusion regions comprises a bond pad material and a via material.

25. (Previously presented) The chip-scale package of claim 24, wherein the diffusion regions at least partially secure the semiconductor device to the interposer.

26. (Previously presented) The chip-scale package of claim 21, further comprising an intermediate layer disposed between the interposer and the semiconductor device.

27. (Previously presented) The chip-scale package of claim 26, wherein the bond pads and the corresponding vias contact each other through the intermediate layer.

28. (Previously presented) The chip-scale package of claim 26, wherein the intermediate layer comprises a material which adheres the semiconductor device to the interposer.

29. (Previously presented) The chip-scale package of claim 26, wherein the intermediate layer comprises a polyimide.

30. (Previously presented) The chip-scale package of claim 21, further comprising at least one conductive bump in communication with at least one conductive via of the corresponding conductive vias, protruding from the interposer opposite from the semiconductor device, and located at an opposite end of the at least one conductive trace from the at least one conductive via.

31. (Previously presented) The chip-scale package of claim 30, wherein the at least one conductive bump comprises solder.

32. (Previously presented) The chip-scale package of claim 21, wherein the interposer comprising semiconductor material and a substrate of the semiconductor device comprise the same material.

33. (Previously presented) The chip-scale package of claim 21, wherein the interposer comprises silicon.

34. (Previously presented) The chip-scale package of claim 21, wherein a substrate of the semiconductor device comprises silicon.

35. (Previously presented) The chip-scale package of claim 21, wherein a first thickness of the interposer and a second thickness of the semiconductor device are substantially equal.

36. (Previously presented) The chip-scale package of claim 21, wherein a first thickness of the interposer is less than a second thickness of the semiconductor device.

37. (Previously presented) The chip-scale package of claim 21, further comprising an insulative material disposed on at least a portion of the second surface of the interposer.

38. (Previously presented) The chip-scale package of claim 37, wherein at least one conductive via of the corresponding conductive vias is exposed through the insulative material.

39. (Previously presented) The chip-scale package of claim 37, wherein the insulative material comprises an oxide.

40. (Previously presented) The chip-scale package of claim 37, wherein the insulative material comprises silicon oxide.

41. (Previously presented) The chip-scale package of claim 37, wherein the insulative material comprises an insulative layer disposed substantially over the second surface.

42. (Canceled)

43. (Currently amended) A flip-chip carrier, comprising an interposer comprising semiconductor material and including:

solder forming at least one via ~~formed therethrough, comprising solder, and having~~ through the interposer and a conductive structure protruding from the at least one via at a first end of the at least one via located proximate a first surface of the interposer and positioned to substantially align with a corresponding bond pad of a semiconductor device to be positioned adjacent to the first surface of the interposer; and

at least one conductive trace laterally extending from a second end of the at least one via and carried by a second surface of the interposer, which is located opposite the first surface of the interposer.

44. (Previously presented) The flip-chip carrier of claim 43, wherein the at least one via comprises an electrically conductive material.

45. (Previously presented) The flip-chip carrier of claim 43, further comprising an insulative material disposed on at least a portion of at least one surface of the interposer.

46. (Previously presented) The flip-chip carrier of claim 45, wherein the insulative material comprises an oxide.

47. (Previously presented) The flip-chip carrier of claim 45, wherein the insulative material comprises silicon oxide.

48. (Previously presented) The flip-chip carrier of claim 45, wherein the insulative material comprises an insulative layer disposed substantially over the at least one surface.

49. (Previously presented) The flip-chip carrier of claim 45, wherein the at least one via is exposed through the insulative material.

50. (Previously presented) The flip-chip carrier of claim 43, wherein the interposer comprises silicon.

51. (Previously presented) The flip-chip carrier of claim 43, further comprising a conductive bump disposed adjacent an end of the at least one conductive trace located opposite from the second end of the at least one via.

52. (Previously presented) The flip-chip carrier of claim 51, wherein the conductive bump comprises solder.

53. (Previously presented) The flip-chip carrier of claim 43, further comprising an adhesive layer disposed adjacent the first surface of the interposer.

54. (Previously presented) The flip-chip carrier of claim 53, wherein the adhesive layer comprises a polyimide.

55. (Previously presented) The flip-chip carrier of claim 53, wherein the first end of the at least one via extends through the adhesive layer.

56-72. (Canceled)